Approved
TP
2/12/04

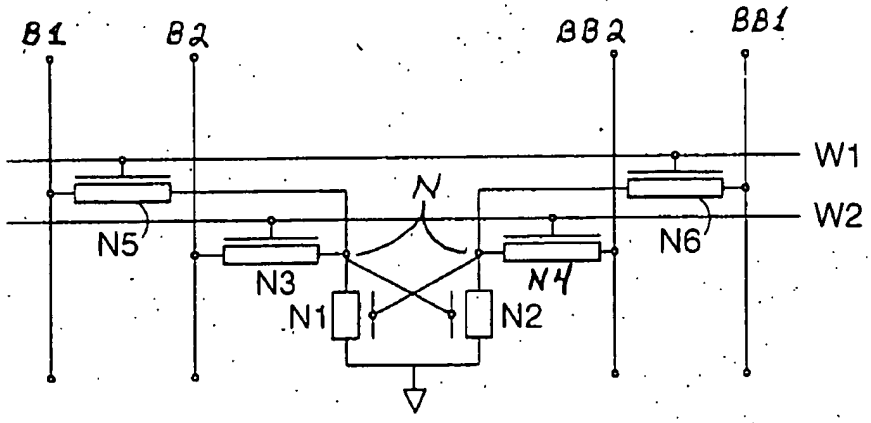


FIG. 1A

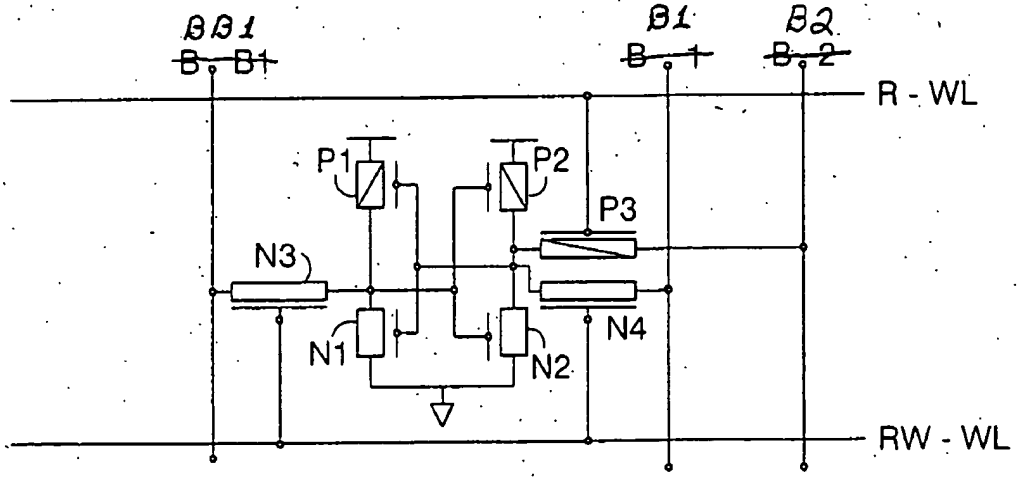
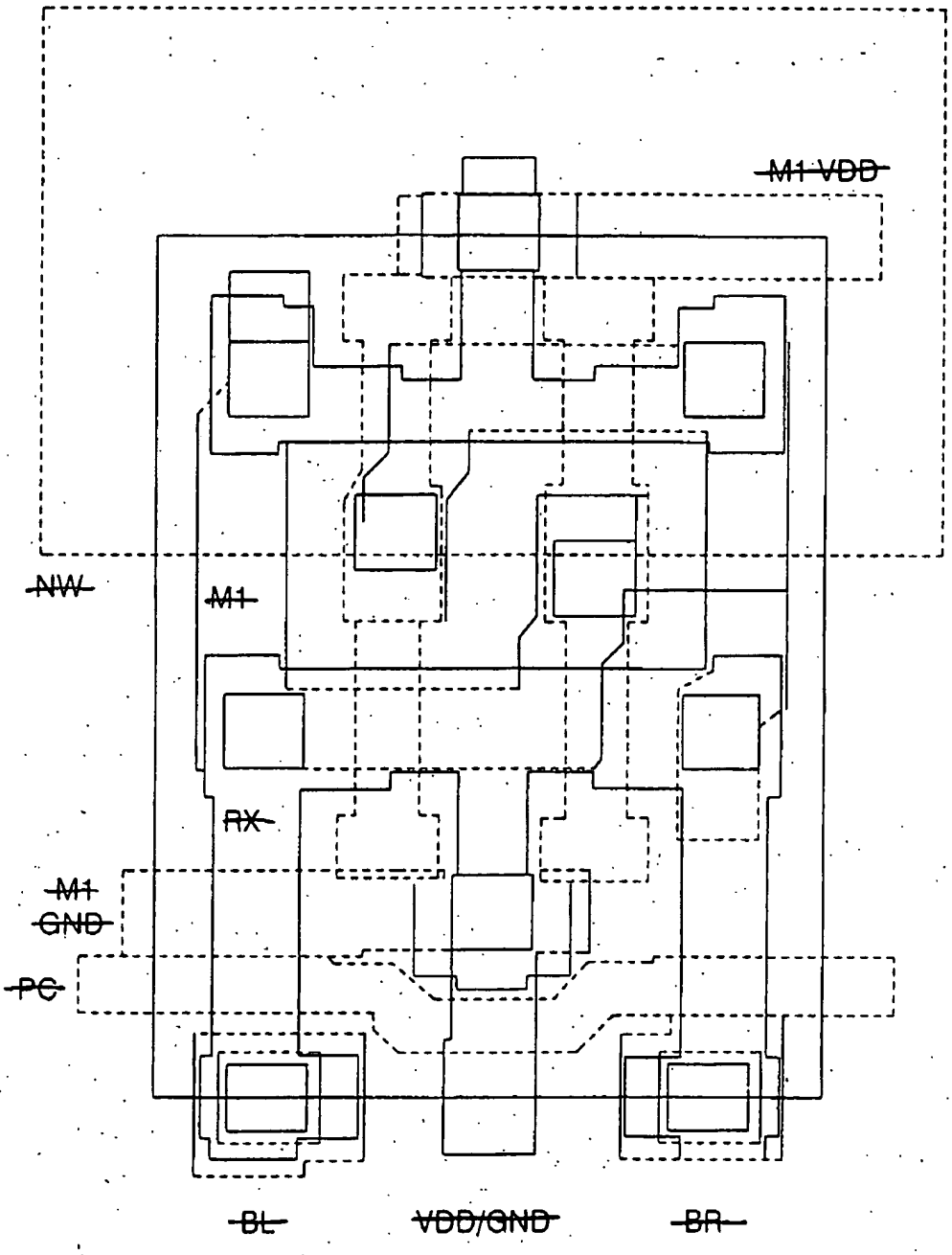
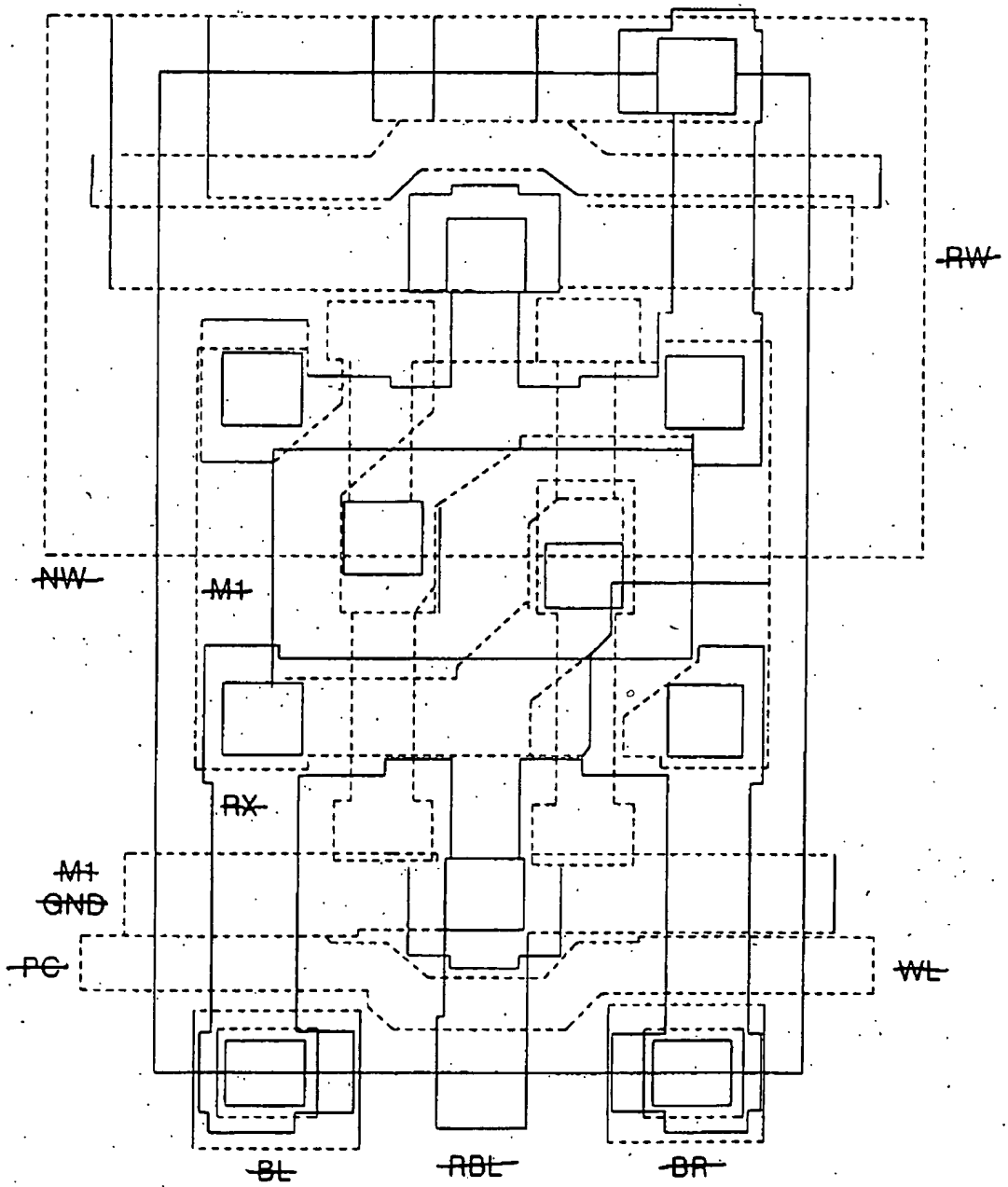


FIG. 1B



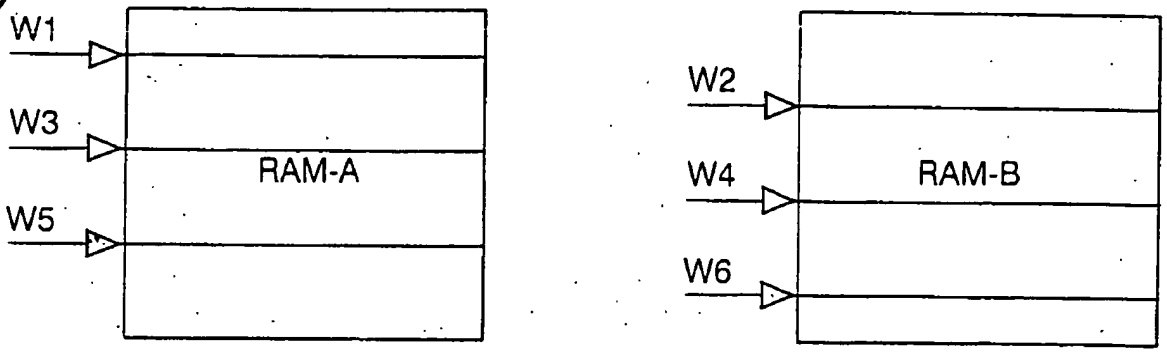
1 Port SRAM Cell
1.3 x 1.9 - 2.47

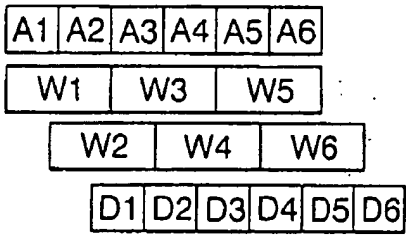
FIG. 1C(1)
(Prior Art)



2 Port SRAM Cell
1.3 x 2.3 - 2.99 ~~(1.22 x 2.47)~~

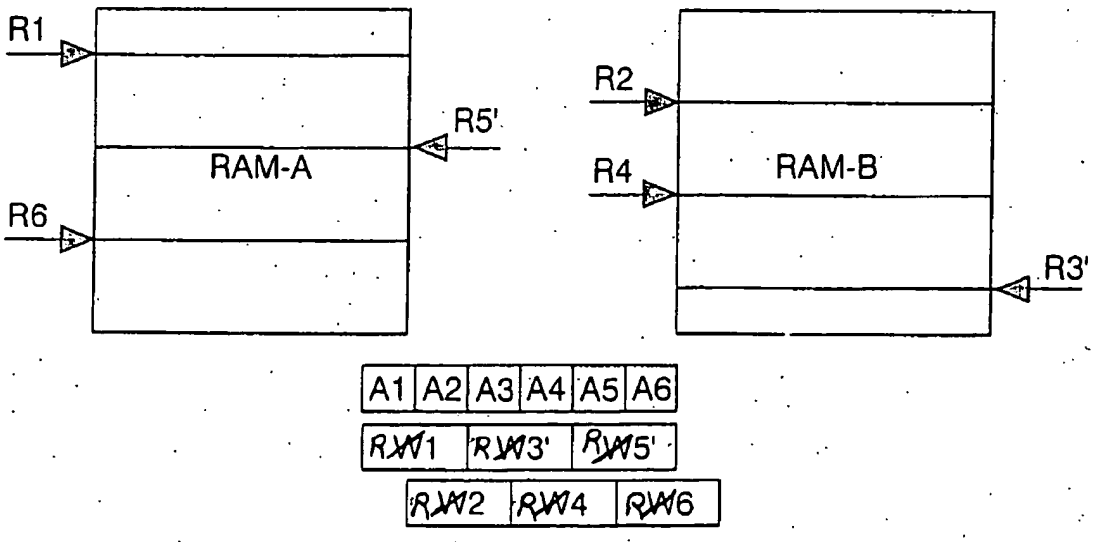
FIG. 1C(2)





Dual-Port RAM, Interleaved Write Operation

FIG. 2



Dual-Port RAM, Interleaved ~~Write~~ Read Operation

FIG. 3